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09/492,265	01/27/2000	Yi-Hsien Hao	34556/JFO/B600	9668

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EXAMINER

PHILPOTT, JUSTIN M

ART UNIT	PAPER NUMBER
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2665

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/492,265

Applicant(s)

HAO ET AL.

Examiner

Justin M Philpott

Art Unit

2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 08 April 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-60 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-60 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 January 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## **DETAILED ACTION**

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Objections***

2. Claims 24 and 58 are objected to because of the following informalities: it appears that “present” (claim 24, page 18, line 20) should be changed to “presenting”; and “The packet-based switch of claim 58” (claim 58, page 23, line 23) should be changed to “The packet-based switch of claim 57”. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 6, 22, 41, 51 and 56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation “the associative memory structure” in claim 1. There is insufficient antecedent basis for this limitation in the claim.

Claims 22, 41, 51 and 56 recite the limitation “the number of memory accesses required per Ethernet frame” in claims 21, 34, 45 and 52, respectively. There is insufficient antecedent

Art Unit: 2665

basis for this limitation in the claim. That is, the structures recited in claims 21, 34, 45 and 52 do not include limitations which state or imply that Ethernet frames are utilized, and therefore, reference to an Ethernet frame format in claims 22, 41, 51 and 56 lacks proper antecedent basis. However, the recitation of "the number of memory accesses required per Ethernet frame" in claim 7 is proper because claim 3, which claim 7 is dependent upon, recites that the switch implements an IEEE Standard 802.3 communication protocol, which by definition of the IEEE 802.3 Standard implies that Ethernet frames are utilized. Accordingly, Applicant may overcome this rejection to claims 22, 41, 51 and 56 by, e.g., amending claims 21, 34, 45 and 52 to include the limitation that the structure implements an IEEE Standard 802.3 communication protocol.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-4, 6, 8, 9, 11, 13-15, 18-21, 23-25, 28-30, 32-34, 37-40, 42-44, 47, 48, 52, 53 and 57-60 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,021,132 to Muller et al.

Regarding claims 1, 8, 9, 11, 13, 15, 21, 28, 32-34, 40, 52 and 57, Muller teaches a memory structure (e.g. see FIG. 1 and col. 3, line 52 – col. 7, line 40) comprising an Address

Art Unit: 2665

Resolution Table (e.g., address table stored in forwarding memory 113, see col. 4, lines 32-34) for resolving addresses in a packet-based network switch (101); and a Packet Storage Table (e.g., shared memory manager 220 locally storing pointers which point to buffers that contain packet data, see col. 6, lines 43-63) adapted to receive a packet for storage in the packet-based network switch and sharing a preselected portion of memory with the Address Resolution Table, wherein Address Resolution Table utilizes a preselected portion of memory comprising the forwarding and filtering database 140 (FIGS. 1 and 2). Furthermore, regarding claims 8, 13, 32, 52 and 57, Muller teaches the Address Resolution Table (113) has an associative memory structure (e.g., associative memory 114 within database 140 and further coupled to switch fabric 210). Still further, regarding claims 8, 9, 13 and 32, Muller teaches the Packet Storage Table is adapted to receive at least one of each of a Packet Data Address (e.g., within the header received from forwarding decision, see col. 5, line 46 – col. 6, line 40) and a Packet Data Value (e.g., a priority indication, see col. 6, line 21). Additionally, regarding claims 11, 33, 52 and 57, Muller teaches the associative memory structure (114) is a direct-mapped/one-way associative memory structure, such that the associative memory structure (114) stores data associated with each entry in the Address Resolution Table (114) (e.g., see col. 4, lines 30-37).

Regarding claims 2, 18 and 37, Muller further teaches the structure comprises a Transmit Descriptor Table (e.g., output queue, see col. 7, lines 20-25) being associated with a corresponding packet-based network transmit port (output port 206); and a Free Buffer Pool (e.g., shared memory 230 comprising free pool of buffers, see col. 7, lines 25-67) having plural memory buffers each having a pre-determined number of memory locations (e.g., memory lines) associated therewith (e.g., see col. 8, lines 37-51).

Art Unit: 2665

Regarding claims 3, 29, 47 and 59, Muller teaches the structure implements an IEEE Standard 802.3 communication protocol (e.g., see col. 3, lines 57-62).

Regarding claims 4, 30, 48, 53 and 60, Muller teaches the switch comprises plural ports (e.g., see FIG. 2 input and output ports 206).

Regarding claims 6, 14 and 58, Muller teaches the associative memory comprises a search structure (e.g., search engine within coupled switch fabric block 210, see col. 6, lines 4-7).

Regarding claims 19, 20, 38 and 39, Muller teaches the Free Buffer Pool further comprises a buffer control memory (e.g., tag array, see col. 9, line 57 – col. 10, line 45) comprising plural memory bits (e.g., represented by rows and columns) uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

Regarding claims 23 and 42, Muller teaches the structure further comprises a free buffer manager (e.g., shared memory manager comprising buffer tracking unit 329 and coupled with switch fabric 210, see FIGS. 2, 3B and 4) including: a buffer bus controller (e.g., buffer manager 325, see col. 9, line 5 – col. 14, line 37), a buffer bus register (e.g., arbitor 470), a buffer control finite state machine (e.g., array controller 450) operably coupled with the bus controller and the bus register, and a buffer search engine (e.g., search engine within block 210, see col. 6, lines 1-23) operably coupled with the bus controller, bus register, and finite state machine.

Regarding claims 24 and 43, Muller teaches the buffer bus controller comprises a buffer free bus controller (performed by buffer manager 325) for detecting a buffer request (Br\_Ptr\_IP-Bus Request) and presenting the request to at least one of the finite state machine and the buffer search engine (e.g., see col. 13, lines 5-14), and a buffer grant bus controller (performed by

Art Unit: 2665

buffer manager 325) for granting an available free buffer (Br\_Ptr\_Data\_BM\_to\_IP[X:0]) as indicated by the buffer bus register (e.g., see col. 13, lines 15-23).

Regarding claims 25 and 44, Muller teaches the buffer search engine comprises a pipelined buffer search engine by coupling learning logic (e.g., see col. 6, line 5) to the search engine for searching and maintaining the database 140.

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 5, 7, 10, 12, 16, 17, 22, 26, 27, 31, 35, 36, 41, 45, 46, 49-51 and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller.

Regarding claims 5, 49, 50, 54 and 55, while Muller may not specifically require that the switch comprise at least 4 ports or at least 8 ports, Muller teaches a plurality of ports are included (e.g., see FIG. 2), and does not limit the scope of the invention to a specific number of ports.

Thus, the teachings of Muller clearly encompass the limitations of providing at least 4 ports or at least 8 ports. Moreover, it is generally considered to be within the ordinary skill in the art to adjust, vary, select or optimize the numerical parameters or values of any system absent a showing of criticality in a particular recited value. The burden of showing criticality is on Appellant. In re Mason, 87 F.2d 370, 32 USPQ 242 (CCPA 1937); Marconi Wireless Telegraph Co. v. U.S., 320 U.S. 1, 57 USPQ 471 (1943); In re Schneider, 148 F.2d 108, 65 USPQ 129

Art Unit: 2665

(CCPA 1945); In re Aller, 220 F.2d 454, 105 USPQ 233 (CCPA 1955); In re Saether, 492 F.2d 849, 181 USPQ 36 (CCPA 1974); In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977); In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 7, 12, 22, 31, 41, 51 and 56, while Muller may not specifically disclose a specific number of memory accesses required per Ethernet frame, it is commonly known in the art to perform, e.g., one cycle per Ethernet frame for operations such as address resolution/learning and transmission read/write.

Regarding claim 10, as discussed above regarding claims 2, 18 and 37, Muller teaches the structure comprises a Transmit Descriptor Table (e.g., output queue, see col. 7, lines 20-25) being associated with a corresponding packet-based network transmit port (output port 206); and a Free Buffer Pool (e.g., shared memory 230 comprising free pool of buffers, see col. 7, lines 25-67) having plural memory buffers each having a pre-determined number of memory locations (e.g., memory lines) associated therewith (e.g., see col. 8, lines 37-51). However, Muller may not specifically disclose receiving a Table Descriptor Address and a Table Descriptor Value at the Transmit Descriptor Table. Nevertheless, Muller clearly suggests that the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value by way of previous example, wherein Muller teaches Address and Value are received by the Packet Storage Table as discussed above regarding claims 8, 9, 13 and 32, and wherein Muller further teaches in steps (1) – (5) (see col. 5, lines 46-65) processing packets from Address Resolution Table (113) to Packet Storage Table (220) to Free Buffer Pool (230) and finally to Transmit Descriptor Table (at output queue 206), thus, clearly suggesting that Address and Value are also received by the Transmit Descriptor Table. Thus, at the time of the invention it would



Art Unit: 2665

have been obvious to one of ordinary skill in the art to adapt the Transmit Descriptor Table of Muller to receive a Table Descriptor Address and a Table Descriptor Value as suggested by Muller by teaching adapting the Packet Storage Table to receive an Address and Value and further teaching steps (1) – (5) wherein packets are processed from Packet Storage Table to Free Buffer Pool and finally to Transmit Descriptor Table.

Regarding claims 16, 17, 35 and 36, while Muller may not specifically require that the Transmit Descriptor Table (output queue) comprise a circular FIFO memory structure with head and tail pointers, such a structure is well known in the art for implementing suitable output queuing, and Muller clearly teaches performing output queuing (output queues at output ports 206).

Regarding claims 26, 27, 45 and 46, while Muller may not specifically require that the buffer bus register comprise an eight-location LIFO, LIFO is a queuing technique well known in the art and Muller clearly teaches performing queuing as discussed above regarding claims 16, 17, 35 and 36.

### *Conclusion*

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,313,582 to Hendel et al. discloses a method and apparatus for buffering data within stations of a communication network,

U.S. Patent No. 5,917,821 to Gobuyan et al. discloses a search engine for a packet-based network,

Art Unit: 2665

U.S. Patent No. 5,938,736 to Muller et al. discloses a search engine architecture for a high performance multi-layer switch element, and

U.S. Patent No. 6,081,522 to Hendel et al. discloses a system and method for a multi-layer network element.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 9:00am-5:00pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703.872.9314 for regular communications and 703.872.9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.4750.

Justin M Philpott



May 19, 2003



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